

**EAST Search History****EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"5678021".pn.	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 09:52
S2	1058	711/152.ccls.	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 10:23
S3	5	("copy" "copying" load\$3) with ( key data secret file information) with ("non-volatile memory" "read only memory" ROM "flash memory" "smart\$1card" thumb USB) same ("write-protected" "wirte-protecting")	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 10:29
S4	19	S2 and ("write-protected" "wirte-protecting")	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 10:46
S5	15	S2 and ("write-protected" "wirte-protecting") and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 10:47
S6	3558	711/163-164,169.ccls.	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 10:55
S7	56	("write-protected" "wirte-protecting") with ( RAM "random access memory" "working memory" "volatile memory") and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 10:57
S8	8	S6 and S7	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 10:57
S9	34	(blocking prevent\$3 ) with ("CPU" "control processing unit") with (writt\$3 modif\$7 chang\$4 alter\$5) with ("RAM" "volatile memory" "working memory")	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 12:01
S10	26	S9 and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 12:01

S11	140	(activat\$3 trigger\$3 start\$3 enabl\$3) with ( blocking preventing ) with ( function signal communication ) with ( "working memory" RAM "read only memory" cache "system memory" "volatile memory")	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 13:15
S12	8	S6 and (activat\$3 trigger\$3 start\$3 enabl\$3) with ( blocking preventing ) with ( function signal communication ) with ( "working memory" RAM "read only memory" cache "system memory" "volatile memory")	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 13:15
S13	5	S12 and @ad<"20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 13:16
S14	97	S11 and @ad<"20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/07 13:18
S15	116	(block\$3 stop\$4 debug\$4 prevent\$3) with ( working near2 memory RAM "random access memory" "volatile memory" cache ) same ((independent seperate) near6 (CPU process))	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 13:09
S16	38	(block\$3 stop\$4 debug\$4 prevent\$3) with ( working near2 memory RAM "random access memory" "volatile memory" cache ) same ((independent seperate) near6 (CPU process)) and @ad<"20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 13:09
S17	725	(blocking stopping debug\$4 prevent\$3) with (CPU "central processing unit") with ( working near2 memory RAM "random access memory" "volatile memory" cache ) and @ad<"20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 13:42

S18	6588	("copy" "copying" load\$3) with ( key data secret file information) with ( mobile phone cellular wireless computer ) with ( portable USB IC SIM card thumb )	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:26
S19	470	("copy" "copying" load\$3) with ( key secret ) with ( mobile phone cellular wireless computer ) with ( portable USB IC SIM card thumb )	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:26
S20	1	S19 and ("write-protected")	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:27
S21	3564	711/163-164,169.ccls.	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:35
S22	13	"711"/\$.ccls. and ("copy" "copying" load\$3) with ( key secret ) with ( mobile phone cellular wireless computer ) with ( portable USB IC SIM card thumb )	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:35
S23	13	"711"/\$.ccls. and ("copy" "copying" load\$3) with ( key secret ) with ( mobile phone cellular wireless computer ) with ( portable USB IC SIM card thumb )	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:36
S24	0	"711"/\$.ccls. and ("copy" "copying" load\$3) with ( key secret ) with ( portable USB IC SIM card thumb ) same (write near2 (protect\$3)) same ("working memory" RAM memory cache)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:39
S25	1	"711"/\$.ccls. and ("copy" "copying" load\$3) same ( key secret ) same ( portable USB IC SIM card thumb ) same (write near2 (protect\$3)) same ("working memory" RAM memory cache)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:39

S26	20	("copy" "copying" load\$3) same ( key secret ) same ( portable USB I C SIM card thumb ) same (write near2 (protect\$3) same ("working memory" RAM memory cache)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:40
S27	8	S26 and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 15:40
S28	72	("copy" "copying" load\$3) with ( key data secret file information) with ("non-volatile memory" "read only memory" ROM "flash memory" "smart\$1card" thumb USB) same (writ\$4 near3(protect\$3 prevent \$3))	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 16:55
S29	44	S28 and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 16:56
S30	4907	"711"/\$.ccls. and (writ\$3 near3 (protect\$3 prevent \$3))	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:03
S31	2297	"711"/\$.ccls. and (writ\$3 near3 (protect\$3 prevent \$3)) with (RAM working near2 memory cache memory)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:05
S32	8	S31 and ((blocking prevent\$3) with ("CPU" "central processing unit") with (writ\$4 modif\$7 chang\$4 alter\$5) with ( RAM "read only memory" "volatile memory" "working memory"))	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:10
S33	5	S32 and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:10
S34	44	S31 and ((blocking prevent\$3) same ("CPU" "central processing unit") same (writ\$4 modif\$7 chang\$4 alter\$5) same ( RAM "read only memory" "volatile memory" "working memory"))	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:21

S35	2407	("copy" "copying" load\$3) with ( key secret information) with (ic smart thumb USB "read only memory" "non-volatile memory") with (computer pc "working memory" "volatile memory" RAM)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:35
S36	1251	(writ\$4 near2 (protect\$4 prevent\$4)) same ((independent separate debugger)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:41
S37	218	(writ\$4 near2 (protect\$4 prevent\$4)) same ((independent separate debugger) with (device unit process))	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:41
S38	218	S36 and S37	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:42
S39	106	S38 and @ad<"20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:42
S40	3564	711/163-164,169.ccls.	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:54
S41	43	S40 and (writ\$4 near2 (protect\$4 prevent\$4)) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:56
S42	19	S41 and @ad<"20030902"	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:56
S43	9	713/193,194.ccls. and (writ\$4 near2 (protect\$4 prevent\$4)) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 17:58
S48	1	711/163-164,169.ccls. and (( writ\$4 near2 (protect\$4 prevent\$4)) with (RAM "working memory" "random access memory" "volatile memory") with (key secret )) and ((prevent\$4 stop\$4 blocking ) with (CPU "central processing unit" "central process unit" debugg\$4 ) with (writ\$3 modif\$7 chang\$4 alter\$5 ) with (Memory))	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 18:11

S49	4	711/163-164,169.ccls. and (( writ\$4 near2 (protect\$4 prevent\$4)) same (RAM "working memory" "random access memory" "volatile memory") same (key secret )) and ((prevent\$4 stop\$4 blocking ) same (CPU "central processing unit" "central process unit" debugg\$4 ) same (writ\$3 modif\$7 chang\$4 alter\$5 ) with (Memory))	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/05/12 18:12
S50	6445	(activat\$3 trigger\$3 start \$3 execut\$3 initiat\$3) near6 (block\$3 prevent\$3 stopp\$3 lock\$3 disabl\$4) with (writ\$4 cop\$4 read\$3 modif\$7 chang\$4 alter\$5) with (RAM random near2 access near2 memory ROM read near2 only near2 memory memory cache) and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 17:01
S51	2650	(activat\$3 trigger\$3 start \$3 execut\$3 initiat\$3) near6 (block\$3 prevent\$3 stopp\$3 lock\$3 disabl\$4) with (writ\$4 cop\$4) near6 (RAM ROM memory cache) and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 17:11
S52	2073	(activat\$3 trigger\$3 start \$3 execut\$3 initiat\$3) near6 (block\$3 prevent\$3 stopp\$3 inhibit\$4 disabl \$4) near6 (writ\$4 cop\$4) near6 (RAM ROM memory cache) and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 17:13
S53	1979	(activat\$3 trigger\$3 start \$3 execut\$3 initiat\$3) near6 (block\$3 prevent\$3 stopp\$3 inhibit\$4 disabl \$4) near6 (writ\$4 copy\$3) near6 (RAM ROM memory cache) and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 17:13

S54	202	(activat\$3 trigger\$3 start \$3 execut\$3 initiat\$3) near6 (block\$3 prevent\$3 stopp\$3 inhibit\$4 disabl \$4) near6 (copy\$3) near6 (RAM ROM memory cache) and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 17:14
S55	70	(activat\$3 trigger\$3 start \$3 execut\$3 initiat\$3) near6 (block\$3 prevent\$3 stopp\$3 inhibit\$4 disabl \$4) near6 (copy\$3) near6 (RAM ROM memory cache) and "711"/\$.ccls. and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 17:20
S56	16	(activat\$3 trigger\$3 start \$3 execut\$3 initiat\$3) near6 (block\$3 prevent\$3 stopp\$3 inhibit\$4 disabl \$4) near6 (cpu "central processing unit" circuit) same (writ\$4 near3 (protect\$4 prevent\$4)) and "711"/\$.ccls. and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 17:46
S57	3	(activat\$3 ) near6 (block \$3 prevent\$3 stopp\$3 inhibit\$4 disabl\$4) near6 (cpu "central processing unit" circuit) same (writ\$4 near3 (protect\$4 prevent \$4)) and "711"/\$.ccls. and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 18:18
S58	43	(activat\$3 ) near6 (block \$3 prevent\$3 stopp\$3 inhibit\$4 disabl\$4) same (writ\$4 near3 (protect\$4 prevent\$4)) and "711"/\$.ccls. and @ad< "20030902"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 18:34
S59	2	"4644494".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	ON	2010/05/13 19:03
S60	1108	711/152.ccls.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	OR	OFF	2010/10/23 15:39

S61	0	S60 and (writ\$4 near2 (protect\$4 prevent\$4)) same (ram working near2 memory volatile near2 memory) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:41
S62	8	711/163.ccls. and (writ\$3 near4 (protect\$4 prevent \$4)) same (ram working near2 memory volatile near2 memory) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:42
S63	1	711/164.ccls. and (writ\$3 near4 (protect\$4 prevent \$4)) same (ram working near2 memory volatile near2 memory) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:42
S64	0	711/169.ccls. and (writ\$3 near4 (protect\$4 prevent \$4)) same (ram working near2 memory volatile near2 memory) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:42
S65	1	713/193.ccls. and (writ\$3 near4 (protect\$4 prevent \$4)) same (ram working near2 memory volatile near2 memory) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:43
S66	1	713/194.ccls. and (writ\$3 near4 (protect\$4 prevent \$4)) same (ram working near2 memory volatile near2 memory) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:43
S67	1	713/189.ccls. and (writ\$3 near4 (protect\$4 prevent \$4)) same (ram working near2 memory volatile near2 memory) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:44
S68	0	726/33.ccls. and (writ\$3 near4 (protect\$4 prevent \$4)) same (ram working near2 memory volatile near2 memory) same ( independent\$3)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:45
S69	0	726/33.ccls. and ( independent\$3) with ( monitoring monitor ) with (copy\$3 near3 data )	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:47

S70	1	713/193.ccls. and ( independent\$3 with ( monitoring monitor ) with (copy\$3 near3 data )	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2010/10/23 15:47
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